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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/526,564 | 03/04/2005 | Takumi Yamaguchi | 67471-065 | 9368 |

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| EXAMINER | |
|---|---|
| LIU, BENJAMIN T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/526,564 | YAMAGUCHI, TAKUMI | |
| | Examiner | Art Unit | |
| | Benjamin T. Liu | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *3/4/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102(b)*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 and 10-11 are rejected under 35 U.S.C 102(b) as being anticipated by Yuzurihara et al. (EP1075028).

With regard to claim 1, figures 1 and 11 of Yuzurihara et al. disclose a solid-state imaging apparatus that includes an imaging region 41 and a drive circuit region 42 both formed on one semiconductor substrate, the imaging region 41 including an active-type unit pixel 41' in which a photodiode unit 1 generates signal charge by photoelectric conversion and an amplification unit 5 amplifies the signal charge, the drive circuit region 42 being for driving the photodiode unit 1 and the amplification unit 5, the imaging region 41 and the drive circuit region 42 including one or more transistors respectively, wherein the transistors in the imaging region 41 and the drive circuit region 42 have a same channel polarity. (Note lines 1-2 in paragraph [0076] of Yuzurihara et al.)

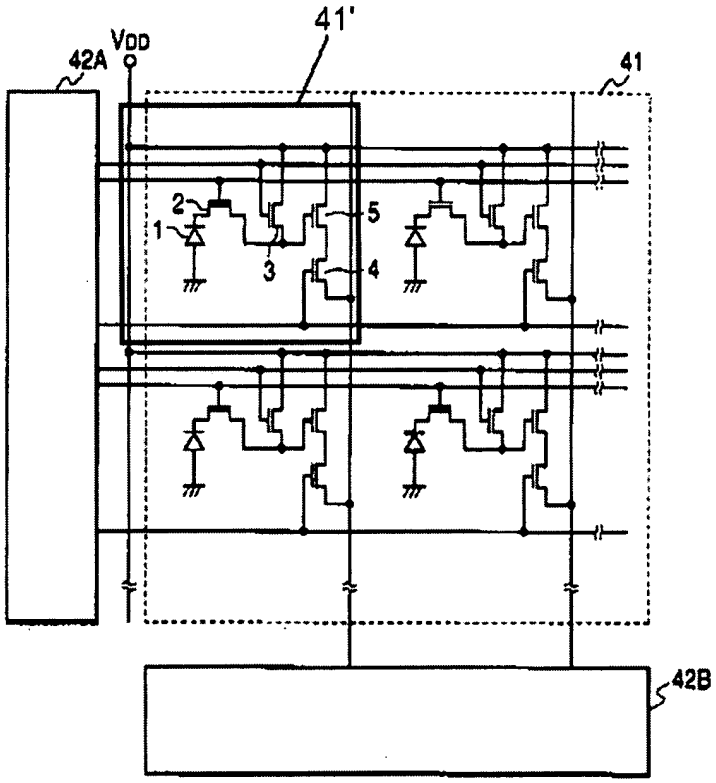


**Figure 1: solid-state imaging apparatus with pixel 41'**

With regard to claim 2, figures 1 and 11 of Yuzurihara et al. disclose a solid-state imaging apparatus, wherein the transistors (2, 3, 4, 5) are of an n-channel MOS type. (Note lines 1-2 in paragraph [0076] of Yuzurihara et al.)

With regard to claim 3, figures 1, 11, and 12 of Yuzurihara et al. disclose a solid-state imaging apparatus, wherein the drive circuit region 42 includes a dynamic circuit that includes a capacitor 7 for accumulating electric charge and a transistor 11 for performing a switching function.

With regard to claim 4, figures 1, 11, and 12 of Yuzurihara et al. disclose a solid-state imaging apparatus, wherein the imaging region 41 includes a plurality of active-

type unit pixels 41', and the drive circuit region 42 includes a pixel selection circuit (42A, 42B) for selecting, one active-type unit pixel 41' from the plurality of active-type unit pixels and a shift resistor circuit for outputting a selection instruction signal to the pixel selection circuit (42A, 42B). (Note lines 5-11 in paragraph [0118] of Yuzurihara et al.)

With regard to claim 5, figures 1, 11, and 12 of Yuzurihara et al. disclose a solid-state imaging apparatus, wherein the imaging region 41 includes a transistor 4 for performing a switching function based on a signal received from the drive circuit region 42, and the signal charge is output to the amplification unit 5 while the transistor 4 for performing the switching function is ON.

With regard to claim 10, figures 1 and 11 of Yuzurihara et al. disclose a manufacturing method for a solid-state imaging apparatus, comprising steps of: forming, on a semiconductor substrate 21, an imaging region 41 including a photodiode unit 1 for converting input light into signal charge and an amplification unit 5 for amplifying the signal charge; and forming, on the semiconductor substrate 21, a drive circuit region 42 for driving the imaging region 41, wherein MOS type transistors having a same channel polarity are formed in both steps for forming the imaging region 41 and the drive circuit region 42 respectively. (Note lines 1-2 in paragraph [0076] of Yuzurihara et al.)

With regard to claim 11, figures 1 and 11 of Yuzurihara et al. disclose a manufacturing method for a solid-state imaging apparatus, wherein the MOS type transistors (1, 2, 3, 4, 5, 42') formed in the both steps are of n-channel MOS type. (Note lines 1-2 in paragraph [0076] of Yuzurihara et al.)

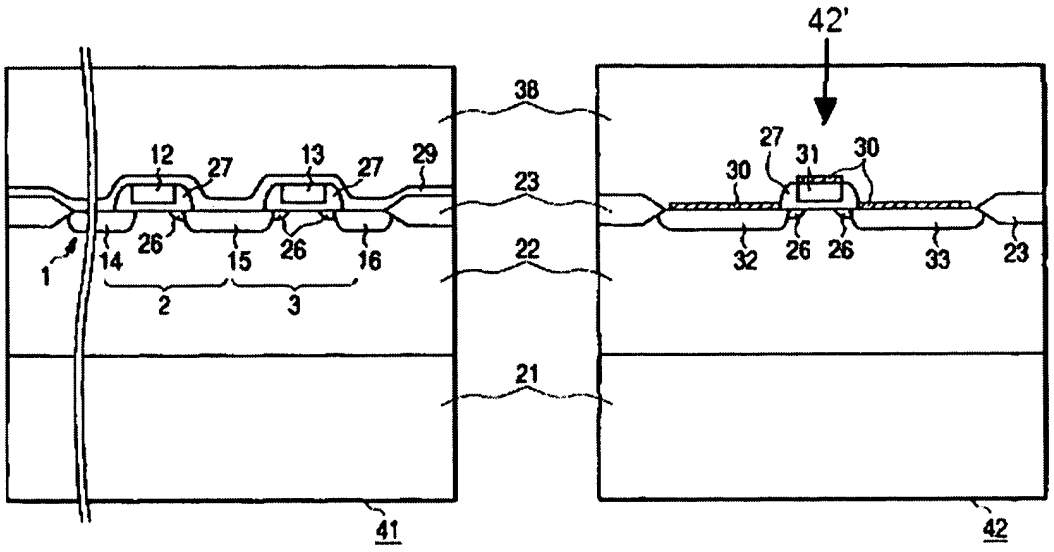


**Figure 2: Peripheral circuit MOS type transistor 42'**

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-8 and 12-14 are rejected under 35 U.S.C 103(a) as being unpatentable over Yuzurihara et al. (EP 1075028) in view of Momose et al. (6,642,560).

With regard to claim 6, figures 1, 11, and 12 of Yuzurihara et al. disclose all the subject matter claimed except for a transistor of a MOS type, of which a gate length is equal to or less than 0.6 um.

However, figure 1 of Momose et al. discloses a transistor of a MOS type, of which a gate length is .3um, which is less than .6um. (Note line 10 in the abstract of Momose et al.)

Therefore, it would have been obvious to one of ordinary skill in the art to form the solid-state imaging apparatus of Yuzurihara et al. with the transistors at the gate lengths taught by Momose et al. in order to decrease the size of each MOS transistor.

With regard to claim 7, figures 1, 11, and 12 of Yuzurihara et al. disclose all the subject matter claimed except for a transistor of a MOS type, of which a film thickness of a gate insulator is in a range from 1 nm to 20 nm.

However, figure 1 of Momose et al. discloses a transistor of a MOS type, of which a film thickness of a gate insulator is less than 2.5nm, which is within the range of 1nm to 20nm. (Note lines 6-7 in the abstract of Momose et al.)

Therefore, it would have been obvious to one of ordinary skill in the art to form the solid-state imaging apparatus of Yuzurihara et al. with the transistors of Momose et al. in order to maintain a certain threshold voltage in each transistor.

With regard to claim 8, figures 1, 11, and 12 of Yuzurihara et al. disclose all the subject matter claimed except for a transistor of a MOS type, an insulator that has a film thickness in a range from 1 nm to 20 nm and functions as a capacitor, which is formed between a gate electrode of the transistor and the semiconductor substrate.

However, figure 1 of Momose et al. discloses a transistor of a MOS type, an insulator 3 that has a film thickness of less than 2.5nm, which is in a range from 1nm to 20nm, and which functions as a capacitor, which is formed between a gate electrode 2 of the transistor and the semiconductor substrate 1. (Note lines 6-7 in the abstract of Momose et al.)

Therefore, it would have been obvious to one of ordinary skill in the art to form the solid-state imaging apparatus of Yuzurihara et al. with the transistors of Momose et al. in order to maintain a certain threshold voltage in each transistor.

With regard to claim 12, figures 1 and 11 of Yuzurihara et al. discloses all the subject matter claimed except for a solid-state imaging apparatus, wherein a gate length of each MOS type transistor is equal to or less than 0.6 pm.

However, figure 1 of Momose et al. discloses a MOS type transistor, wherein a gate length is .3um, which is less than .6um. (Note line 10 in the abstract of Momose et al.)

Therefore, it would have been obvious to one of ordinary skill in the art to form the solid-state imaging apparatus of Yuzurihara et al. with the transistors of Momose et al. in order to crate a solid-state imaging apparatus with small transistors.

With regard to claim 13, figures 1 and 11 of Yuzurihara et al. discloses all the subject matter claimed except for a solid-state imaging apparatus, wherein a film thickness of a gate insulator in each MOS type transistor is in a range from 1 nm to 20 nm.

However, figure 1 of Momose et al. discloses a transistor, wherein a film thickness of a gate insulator in each MOS type transistor is less than 2.5 nm, which is in a range from 1 nm to 20 nm. (Note lines 6-7 in the abstract of Momose et al.)

Therefore, it would have been obvious to one of ordinary skill in the art to form the solid-state imaging apparatus of Yuzurihara et al. with the transistors of Momose et al. in order to form the solid-state imaging apparatus with transistors that have a certain threshold voltage.

With regard to claim 14, figures 1 and 11 of Yuzurihara et al. discloses all the subject matter claimed except for a solid-state imaging apparatus, wherein an insulator that has a film thickness in a range from 1 nm to 20 nm, and functions as a capacitor is formed between a gate electrode of each MOS type transistor and the semiconductor substrate.

However, figure 1 of Momose et al. discloses a transistor, wherein an insulator that has a film thickness of less than 2.5 nm, which is in a range from 1 nm to 20 nm, and functions as a capacitor is formed between a gate electrode 2 of each MOS type transistor and the semiconductor substrate 1.

Therefore, it would have been obvious to one of ordinary skill in the art to form the solid-state imaging apparatus of Yuzurihara et al. with the transistors of Momose et al. in order to form solid-state imaging apparatus with transistors that have a certain threshold voltage.

Claim 9 is rejected under 35 U.S.C 103(a) as being unpatentable over Yuzurihara et al. (EP 1075028) in view of Shinohara et al. (5,698,844).

With regard to claim 9, figures 1, 11, and 12 of Yuzurihara et al. disclose all the subject matter claimed except for a camera that includes the solid-state imaging apparatus.

However, figure 1 of Shinohara et al. discloses a solid-state imaging apparatus that is included in a camera. (Note lines 9-10 in column 1 of Shinohara et al.)

Therefore, it would have been obvious to one of ordinary skill in the art to form the solid-state imaging apparatus of Yuzurihara et al. inside the camera of Shinohara et al. in order to be used as the line sensor for an image scanner and an area sensor for the camera.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin T. Liu whose telephone number is (571) 272-6009. The examiner can normally be reached on Mon-Fri 9:30 AM-6:00AM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BTL